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October 2014

FMS6364A
Four-Channel Standard- & High-Definition (SD & HD) VoltagePlus™ Video Filter Driver

Features

- Three 7th-Order 32 MHz (HD) Filters
- One 6th-Order 8 MHz (SD) Filter
- Drives Single AC- or DC-Coupled Video Loads (150 Ω)
- Drives Dual AC- or DC-Coupled video Loads (75 Ω)
- Transparent Input Clamping
- Single Supply: 3.3 V – 5.0 V
- AC- or DC-Coupled Inputs and Outputs
- DC-Coupled Output Eliminates AC-Coupling Capacitor
- Robust 9kV ESD Protection
- Lead-Free TSSOP-14 Package

Applications

- Cable Set-Top Boxes
- Satellite Set-Top Boxes
- DVD Players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

The FMS6364A VoltagePlus™ video filter is intended to replace passive LC filters and drivers with a cost-effective integrated device. Three 7th-order filters provide HD quality and a single 6th-order SD channel provides compatibility. The FMS6364A may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required *(see the Application Information section for details)*.

The outputs can drive AC- or DC-coupled single (150 Ω) or dual (75 Ω) video loads. DC coupling the outputs removes the need for large output coupling capacitors. The input DC levels are offset approximately +280 mV at the output *(see the Application Information section)*.

Related Resources

AN-6024 – FMS6xxx Product Series; Understanding Analog Video Signal Clamps, Bias, DC Restore, and AC- or DC-Coupling Methods

AN-6041 – PCB Layout Considerations for Video Filter/Drivers

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FMS6364AMTC14X	-40°C to +85°C	14-Lead TSSOP, JEDEC MO-153, 4.4 mm Wide	2500 Units per Reel

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Block Diagram

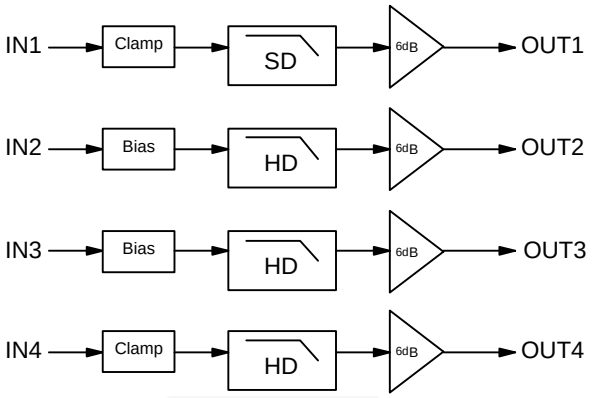

Figure 1. Block Diagram

Pin Configuration

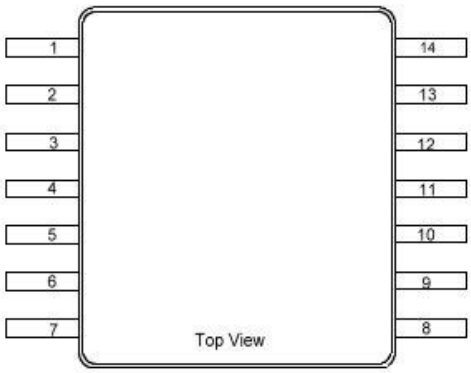

Figure 2. Pin Configuration

Pin Definitions

Pin#	Name	Type	Description
1	IN1	Input	Video Input Channel SD
2	GND	Input	Device Ground Connection
3	IN2	Input	Video Input Channel HD **(Pr)**
4	IN3	Input	Video Input Channel HD **(Pb)**
5	IN4	Input	Video Input Channel HD **(Y)**
6	NC		No Connection
7	V_{CC}	Power	Positive Power Supply
8	GND	Ground	Device Ground Connection
9	NC		No Connection
10	OUT4	Output	Filtered Output Channel HD **(Y)**
11	OUT3	Output	Filtered Output Channel HD **(Pb)**
12	OUT2	Output	Filtered Output Channel HD **(Pr)**
13	GND	Ground	Device Ground Connection
14	OUT1	Output	Filtered Output Channel SD

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_S	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V
I_{OUT}	Maximum Output Current, Do Not Exceed		50	mA

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			150	°C
T_{STG}	Storage Temperature Range	-65		150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			300	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		115		°C/W

Electrostatic Discharge Protection (ESD)

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	IEC61340-3-1:2002 Level II	9	kV
CDM	Charged Device Model ESD	JESD22-C101-A Level III	2	kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		85	°C
V_{CC}	Supply Voltage Range	3.135	3.300	5.250	V

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DC Electrical Characteristics

Unless otherwise noted, T_A=25°C, V_{CC}=3.3 V, R_S=37.5 Ω, all inputs are AC coupled with 0.1 µF, and all output AC coupled with 220 µF into 150 Ω load.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Supply						
V_S	Supply Voltage Range	V_S Range	3.135	3.300	5.250	V
I_{CC}	Quiescent Supply Current(1)	V_S=+3.3 V, No Load, EN=LOW		50	65	mA
		V_S=+5.25 V, No Load, EN=LOW		55	76	mA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC Coupled		1.4		V_{PP}
PSRR	Power Supply Rejection Ratio	DC (All Channels)		-50		dB

Note:
1. 100% tested at T_A=25°C.

Standard-Definition Electrical Characteristics

Unless otherwise noted, T_A=25°C, V_{IN}=1 V_{PP}, V_{CC}=5 V, R_{SOURCE}=37.5 Ω, all inputs AC coupled with 0.1 µF, all outputs AC coupled with 220 µF into 150 Ω loads, and referenced to 400 kHz.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV_{SD}	Channel Gain(2)	All SD Channels	5.8	6.0	6.2	dB
f_{01dBSD}	-0.1 dB Flatness	All SD Channels		5		MHz
f_{1dBSD}	-1 dB Flatness(2)	All SD Channels	7	8		MHz
f_{cSD}	-3 dB Bandwidth(2)	All SD Channels	8	9		MHz
f_{SBSD}	Attenuation (Stopband Reject)(2)	All SD Channels at f=27 MHz	45	60		dB
DG	Differential Gain	All SD Channels		0.3		%
DP	Differential Phase	All SD Channels		0.6		°
THD	Total Harmonic Distortion, Output	V_{OUT}=1.4V_{PP}, 3.58 MHz		0.35		%
X_{TALKSD}	Crosstalk (Channel-to-Channel)	1 MHz		-74		dB
SNR	Signal-to-Noise Ratio(3)	NTC-7 Weighting, 100 kHz to 4.2 MHz		76		dB
t_{pdSD}	Propagation Delay	Delay from Input to Output, 4.5 MHz		90		ns
CLG_{SD}	Chroma Luma Gain(2)	f=3.58 MHz (Ref to SD_{IN} at 400 kHz)	95	100	105	%
CLD_{SD}	Chroma Luma Delay	f=3.58 MHz (Ref to SD_{IN} at 400 kHz)		5.5		ns
t_{ON}	Enable Time			1		µs
t_{OFF}	Disable Time			1		µs

Notes:
2. 100% tested at T_A=25°C.
3. SNR=20 • log (714 mV / rms noise).

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High-Definition Electrical Characteristics

Unless otherwise noted, T_A=25°C, V_{CC}=3.3 V, R_S=37.5 Ω, all inputs are AC coupled with 0.1 µF, and all outputs AC coupled with 220 µF into 150 Ω load.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AV	Channel Gain[4]	Active Video Input Range=1 V_{PP}	5.8	6.0	6.2	dB
ΔAV_{24MHz}	Damping at 24 MHz	R_{SOURCE}=75 Ω, R_L=150 Ω	-0.65			dB
ΔAV_{28MHz}	Damping at 28 MHz	R_{SOURCE}=75 Ω, R_L=150 Ω	-1			dB
$BW_{3.0dB}$	-3.0 dB Bandwidth[4]	R_{SOURCE}=75 Ω, R_L=150 Ω	32	34		MHz
$Att_{37.125M}$	Normalized Stopband Attenuation[4]	R_{SOURCE}=75 Ω, f=37.325 MHz		6.5		dB
$Att_{44.25M}$		R_{SOURCE}=75 Ω, f=44.25 MHz		14.5		dB
$Att_{74.25M}$		R_{SOURCE}=75 Ω, f=74.25 MHz	40	44		dB
Att_{78M}		R_{SOURCE}=75 Ω, f=78 MHz	42	46		dB
THD1	Output Distortion (All Channels)	f=10 MHz; V_{OUT}=1.4 V_{PP}		0.4		%
THD2		f=15 MHz; V_{OUT}=1.4 V_{PP}		0.5		
THD3		f=22 MHz; V_{OUT}=1.4 V_{PP}		0.5		
X_{talk}	Crosstalk (Channel-to-Channel)	f=1.00 MHz; V_{OUT}=1.4 V_{PP}		-70		dB
SNR	Peak Signal to RMS Noise	Unweighted: 30 MHz Lowpass, 100 kHz to 30 MHz		70		dB
t_{pd}	Propagation Delay	Delay from Input to Output; 100 kHz to 26 MHz		25		ns

Note:

4. 100% tested at 25°C.

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Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 3.3 V, R_S = 37.5 Ω, and AC-coupled output into 150 Ω load.

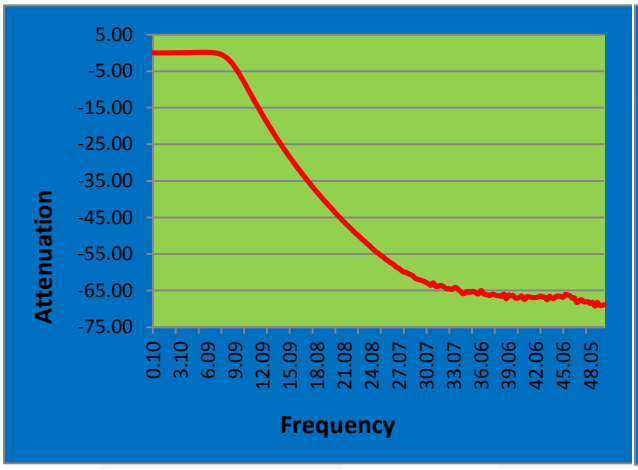


Figure 3. SD Frequency Response

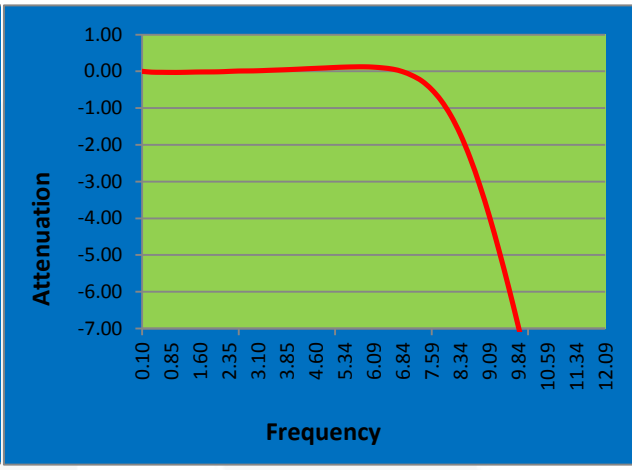


Figure 4. SD Flatness

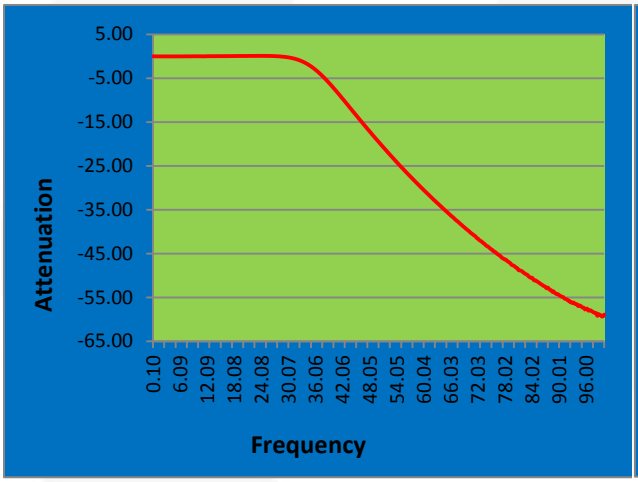


Figure 5. HD Frequency Response

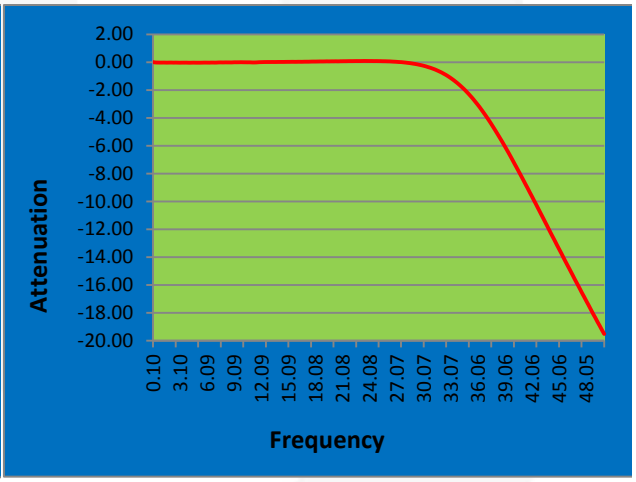


Figure 6. HD Flatness

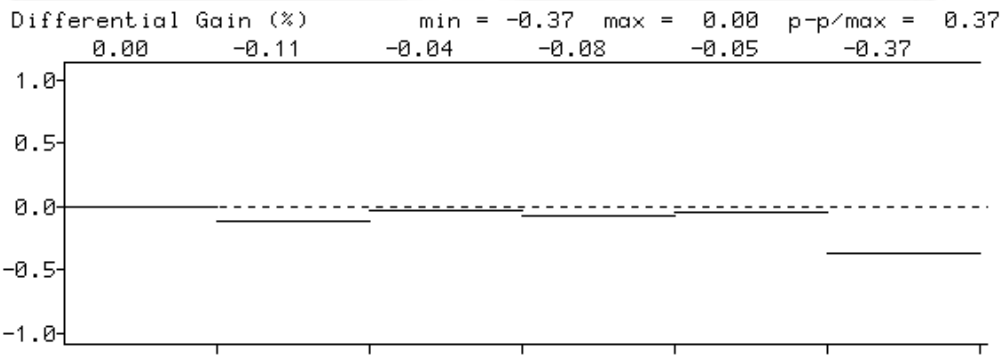


Figure 7. Differential Gain

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 3.3 V, R_S = 37.5 Ω, and AC-coupled output into 150 Ω load.

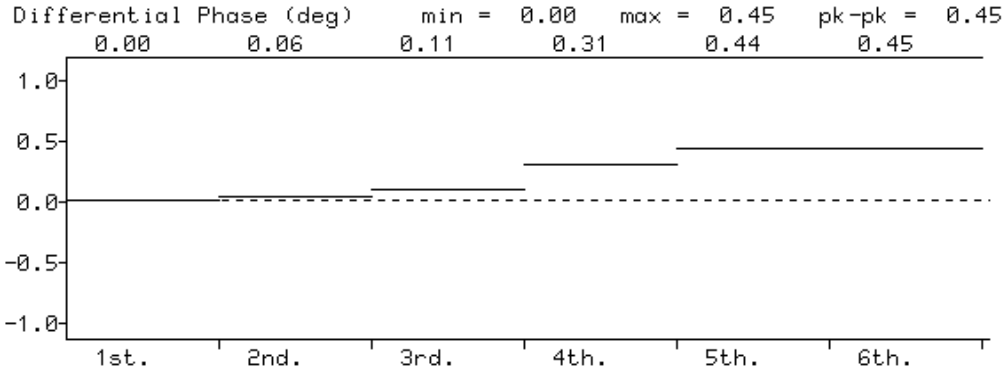


Figure 8. Differential Phase

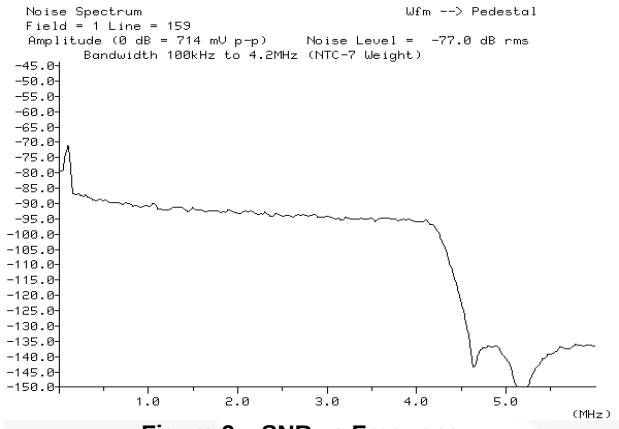


Figure 9. SNR vs Frequency

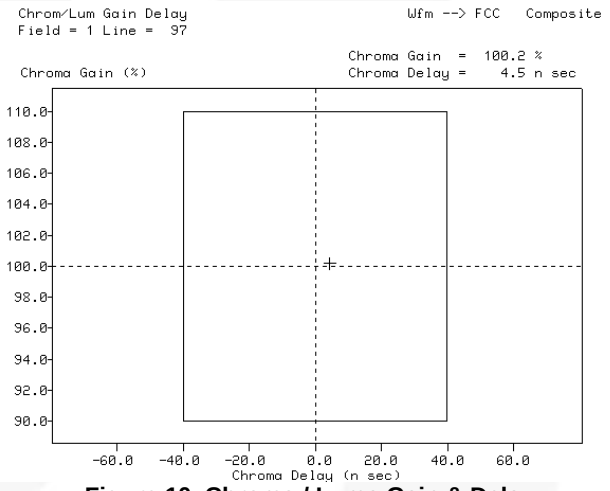


Figure 10. Chroma / Luma Gain & Delay

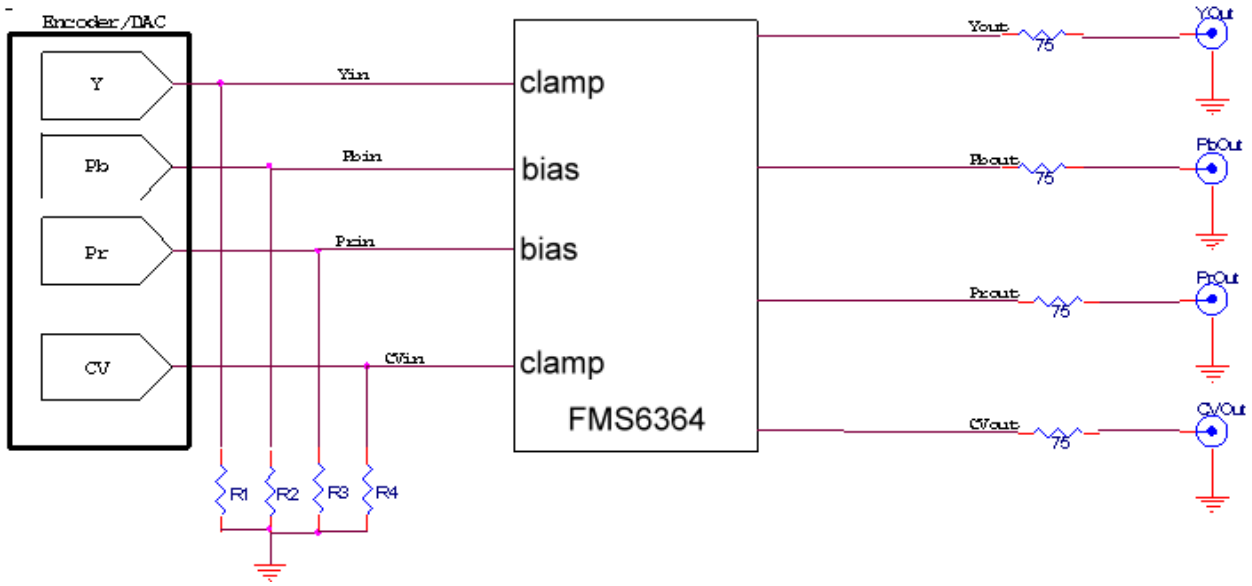
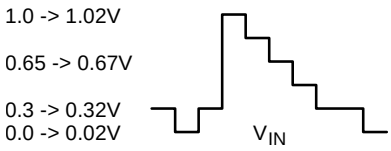


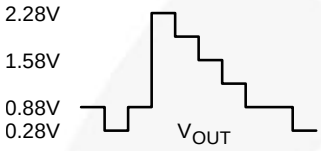
Figure 11. Typical Application

Application Information

Application Circuits

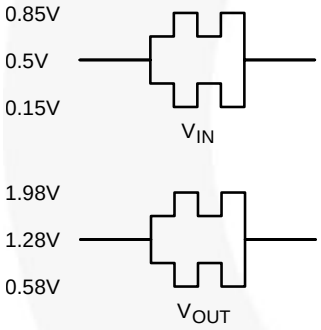
The FMS6364A VoltagePlus™ video filter provides a 6 dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in the diagram below:





Driven by:
DC-Coupled DAC Outputs
AC-Coupled and Clamped
Y, CV, R, G, B

There is a 280mV offset from the DC input level to the DC output level. $V_{OUT} = 2 * V_{IN} + 280mV$.



Driven by:
AC-Coupled and Biased
U, V, Pb, Pr, C

Figure 12. Typical Voltage Levels

The FMS6364A provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6364A without an AC-coupling capacitor. When the input is AC-coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground. The worst-case sync tip compression due to the clamp cannot exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range.

For symmetric signals like Chroma, U, V, Pb, and Pr; the average DC bias is fairly constant and the inputs can be AC coupled. DAC outputs can also drive these same signals without the AC-coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 13:

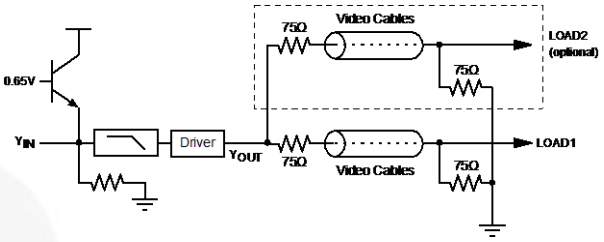


Figure 13. Input Clamp Circuit

I/O Configurations

For a DC-coupled DAC drive with DC-coupled outputs, use the configuration in Figure 14.

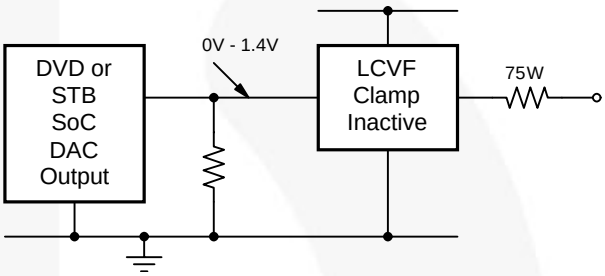


Figure 14. DC-Coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0 V to 1.4 V, it can be AC coupled as shown in Figure 15.

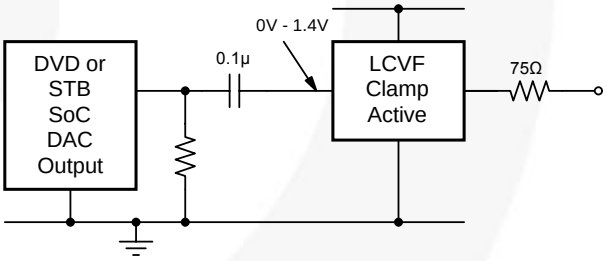


Figure 15. AC-Coupled Inputs, DC-Coupled Outputs

When the FMS6364A is driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC coupled as shown in Figure 16.

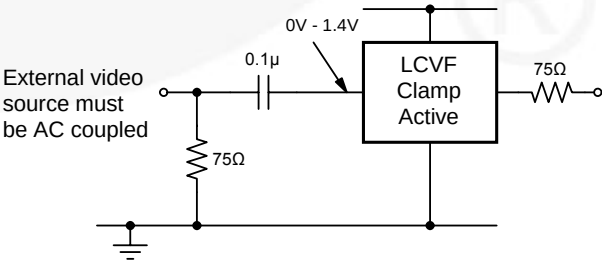


Figure 16. SCART with DC-Coupled Outputs

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The same method can be used for biased signals. The Pb and Pr channels are biased to set the DC level to 500 mV.

The same circuits can be used with AC-coupled outputs if desired.

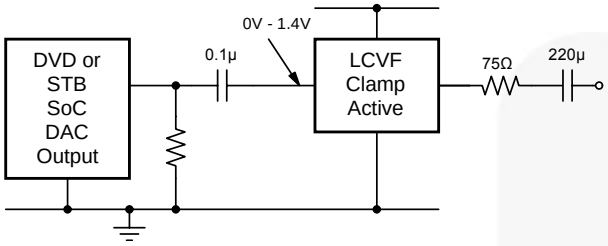

Figure 17. AC-Coupled Inputs and Outputs

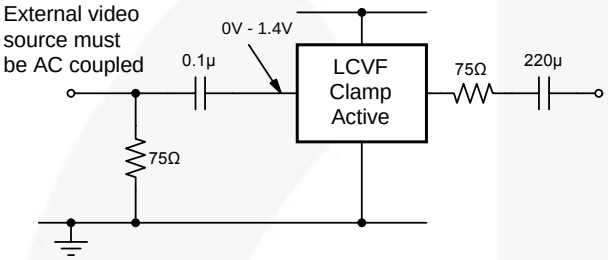

Figure 18. Biased SCART with AC-Coupled Outputs

Note:

5. The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220 µF to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6364A output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following equations can be used to calculate the power dissipation and internal temperature rise.

$$T_J = T_A + P_D \bullet \Theta J_A \quad (1)$$

where:

$$P_D = P_{CH1} + P_{CH2} + P_{CH3} \text{ and} \quad (2)$$

$$P_{CHx} = V_{CC} \bullet I_{CH} - (V_O^2/R_L) \quad (3)$$

where:

$$V_O = 2\ V_{IN} + 0.280\ V \quad (4)$$

$$I_{CH} = (I_{CC}/3) + (V_O/R_L) \quad (5)$$

V_{IN} = RMS value of input signal

I_{CC} = 50 mA

V_{CC} = 3.3 V

R_L = channel load resistance.

Board layout can also affect thermal characteristics. *Refer to the Layout Considerations section for details.*

The FMS6364A is specified to operate with output currents typically less than 50 mA, more than sufficient for a dual (75 Ω) video load. Internal amplifiers are current limited to a maximum of 100 mA and should withstand brief-duration short-circuit conditions. This capability is not guaranteed.

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Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board to guide layout and aid device evaluation. The demo board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing/Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Do not run traces on top of the ground plane.
- Run no traces over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 0.01 µF and 0.1 µF ceramic power supply bypass capacitors.
- Place the 0.1 µF capacitor within 2.54 mm (0.1 in) of the device power pin.
- Place the 0.01 µF capacitor within 19.05 mm (0.75 in) of the device power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body at least 12.7 mm (0.5 in) on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.
- Place a 75 Ω series resistor within 12.7 mm (0.5 in) of the output pin to isolate the output driver from board parasitics.

Output Considerations

The FMS6364A outputs are DC offset from the input by 150 mV; therefore V_{OUT} = 2 • V_{IN} DC+150 mV. This offset is required to obtain optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6364A has a 2 x (6 dB) gain, the output is typically connected via a 75 Ω-series back-matching resistor followed by the 75 Ω video cable. Because of the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less than 1 V. When AC coupling the output, ensure that the coupling capacitor of choice passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. To obtain the highest quality output video signal, the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the output driver. The distance from device pin to the series termination resistor should be no greater than 12.7 mm (0.5 in).

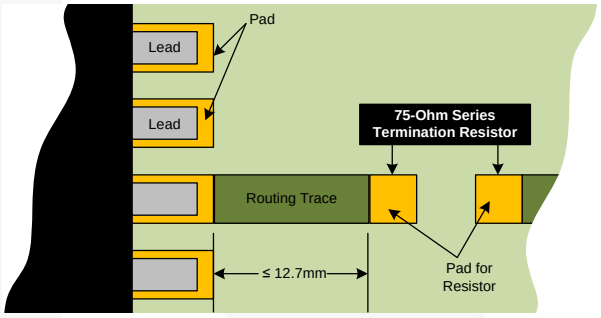

Figure 19. Recommended Resistor Placement

Thermal Considerations

Since the interior of systems such as set-top boxes, TVs, and DVD players are at +70ºC; consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane), each other on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70 µm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in the power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Consider modeling techniques a first-order approximation.

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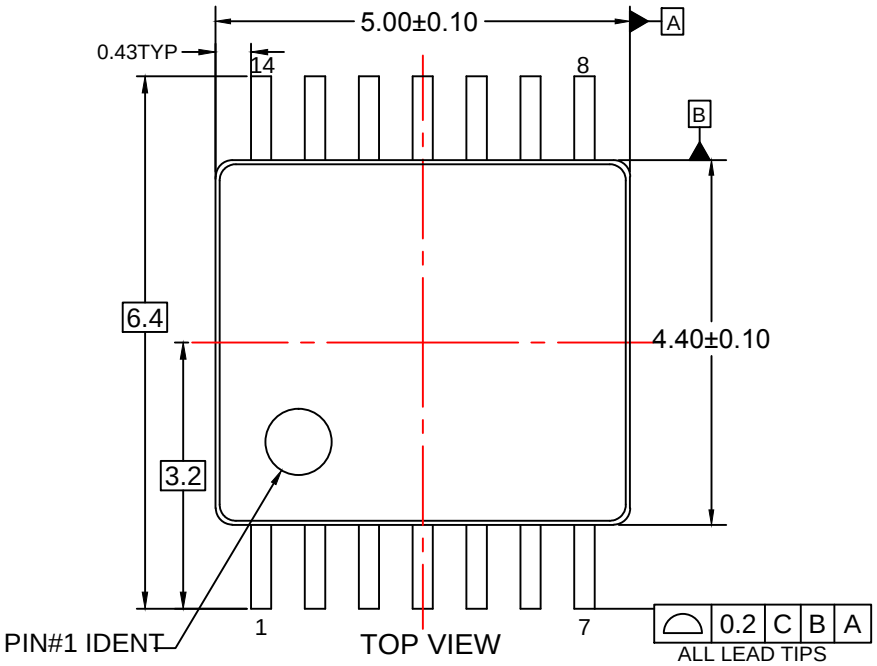
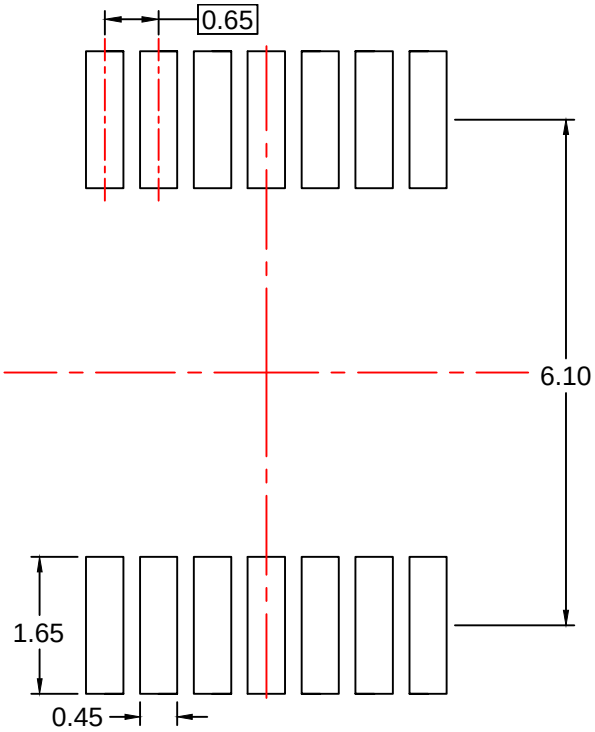
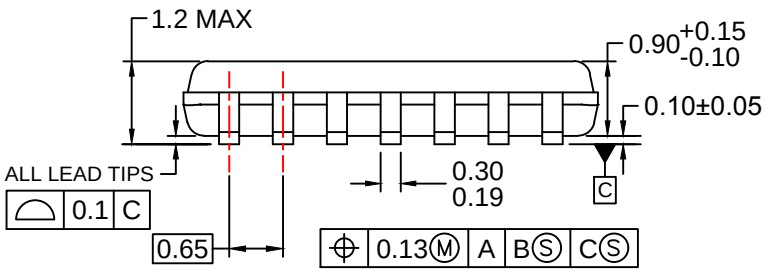


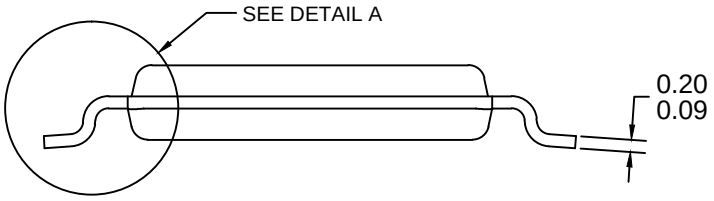
TOP VIEW

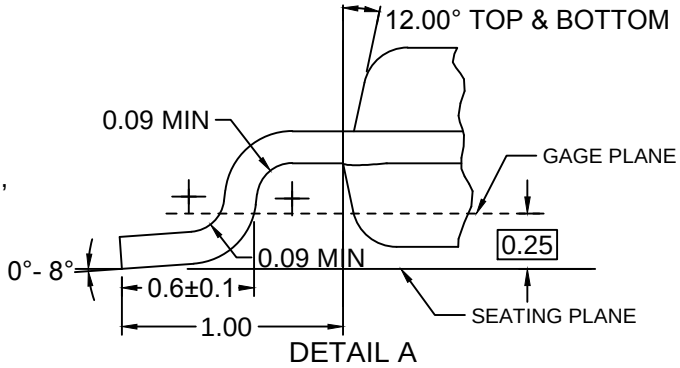


RECOMMENDED LAND PATTERN



FRONT VIEW





DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

E. LANDPATTERN STANDARD: SOP65P640X110-14M.

F. DRAWING FILE NAME: MKT-MTC14rev7.

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